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SS3601 / SS3602

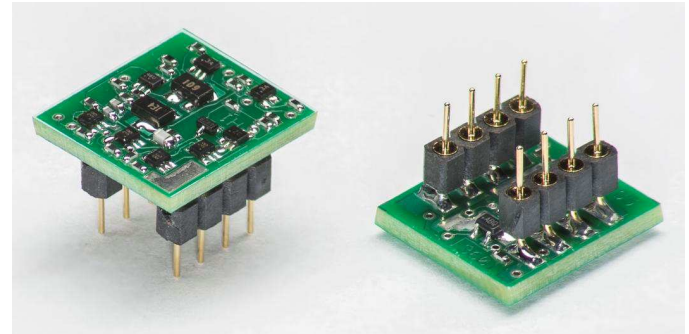
Description :

The SS3601 / SS3602 are single / dual discrete op amps in an 8 pin DIP compatible package optimized for high performance audio applications. These devices are drop in replacements for many common, yet inferior audio operational amplifiers and are uniquely compensated for trouble free swap out into virtually any circuit. Having a footprint of a mere 0.33 square inches, these devices are one-third the size of any other discrete op amp on the market. Class A biasing and high output current capability coupled with a proprietary two pole compensation scheme requiring multiple NPO dielectric capacitors make these discrete op amps impossible to fabricate as a monolithic IC.

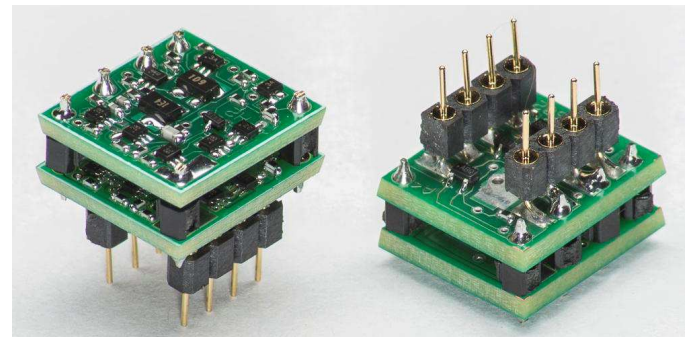
Features:

- **140 dB Open Loop Gain to 600 Hz**
- **Class A Output Current Of +/- 15mA**
- **Maximum Output Current Of +/- 50mA**
- **Extremely Tolerant of Capacitive Loads And High Feedback Network Impedance**
- **Trouble Free Drop In Replacement For Audio Op amps**
- **Smallest Discrete Op Amp On The Market**
- **DIP 8 Compatible Package**
- **Fully Discrete Design**
- **True Op Amp Requiring No Ground For Normal Operation**

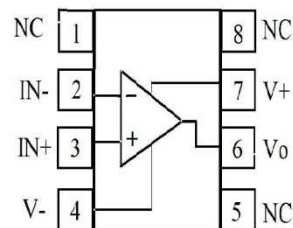
Single Discrete Op amp SS3601



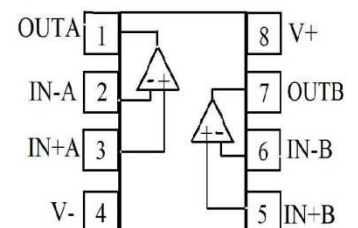
Dual Discrete Op Amp SS3602



PIN ASSIGNMENT



SS3601 SINGLE



SS3602 DUAL

Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings could result in permanent damage to the device. These ratings are absolute maximum, and are not recommended for normal operation.

Symbol	Parameter	Conditions	Rating	Unit	Notes
Vcc	Supply Voltage	Single Supply	44	V	
		Split Supply	±22		
Vdiff	Sustained Differential Input Voltage		680	mV	4
Vcm	Common Mode Input Voltage		Vcc to Vee	V	
Iin	Input Current	+ or - op amp input	50	mA	4
Io	Output Current	Short to Ground	50	mA	1, 2
		Short to Vcc or Vee	50	mA	1, 3
Top	Operating Ambient Temperature		-25 to +70	°C	
Tstg	Storage Temperature		-40 to +120	°C	

Notes:

- The output current is internally limited
- Short circuits to ground can be maintained indefinitely
- Short circuits to Vcc or Vee may damage the device by overheating if they are prolonged for several seconds
- The input pins are clamped with back to back (anti parallel) schottkey diodes.

DC Characteristics

Unless otherwise noted, Ta = 25°C, Vcc = +12V, Vee = - 12V, Vcm = 0

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
Vcc	Supply Voltage	Single Supply	12	24	36	V	
		Split Supply	±6	±12	±18	V	
Iq	Quiescent Current	SS3601 Single	13.5	14.5	15.5	mA	1
		SS3602 Dual	26	27.5	28	mA	1
Vos	Input Offset Voltage			±300	±600	µV	
Vcm	Common Mode Input Voltage		Vee + 3		Vcc - 3	V	
Ib	Input Bias Current			4.5	6	µA	
Io	Output Current	Class A Mode		15		mA	2
		Class AB Mode		40		mA	3
		Current Limit		50	65	mA	

Notes:

- Quiescent current is supply voltage dependent, and is graphed in the Typical Performance Characteristics section of this data sheet.
- This is the Max Io that the output stage can swing while remaining in class A mode
- This is the Max Io that the output stage can swing without entering current limit

AC Characteristics

Unless otherwise noted, $T_a = 25^\circ\text{C}$, $V_{cc} = +15\text{V}$, $V_{ee} = -15\text{V}$, $V_{cm} = 0$

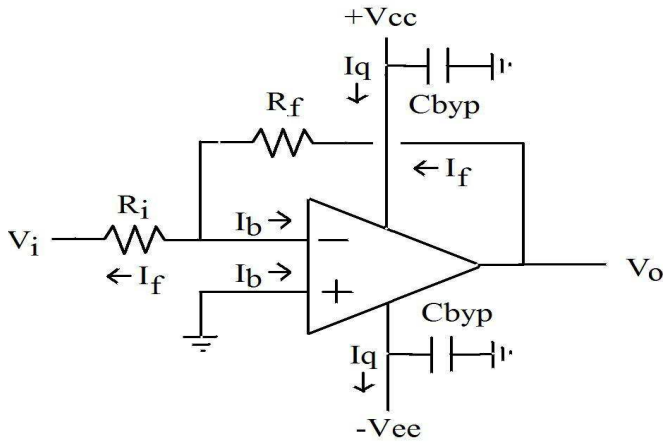
Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
Aol	Open Loop Gain			140		dB	1
SR	Slew Rate	Positive Direction		20		V/ μS	
		Negative Direction		12		V/ μS	
Vo max	Maximum Output Voltage	@ Minimum THD	Vee+3.5		Vcc-3.5		4
		@ clip	Vee+1.5		Vcc-1.5		
Cl	Capacitive Load Drive	Figure 1 or 2, $A_v = -1$ or $+2$		2500		pF	2
Cl	Capacitive Load Drive	Figure 4, $A_v = +1$		500		pF	2
BW	Unity Gain Bandwidth			5		MHz	1
θ_m	Phase Margin	@ Unity gain Crossover		75		$^\circ$	1
CT	Cross Talk	Amplifier to Amplifier	100		120	dB	5
en	Voltage Noise Density	DC - 20 KHz Bandwidth		2.9		nV/ $\sqrt{\text{Hz}}$	
N	Broad Band Noise	DC - 20 KHz Bandwidth		415		nV RMS	
Cin	Input Capacitance			5		pF	

Notes

- 1 A plot of Open Loop Gain and Phase across frequency can be found in the Typical Performance Characteristics section of this datasheet.
- 2 This specification does not apply to capacitors inside of the external feedback loop, such as in filter circuits, as these will not affect stability.
- 3 For more information, see the Applications Section of this data sheet.
- 4 Cascode structures inside of the device will begin to debias when the output swing approaches 3.5V away from either supply rail. This is non destructive, and the output will not visibly clip, however there will be a $\sim 25\text{dB}$ reduction in open loop gain, resulting in higher THD.
- 5 This specification applies to the SS3602 Dual Pack device only.

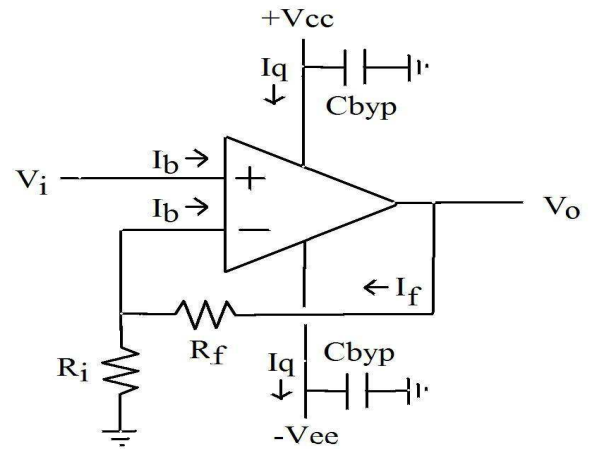
Application Circuits

Figure 1



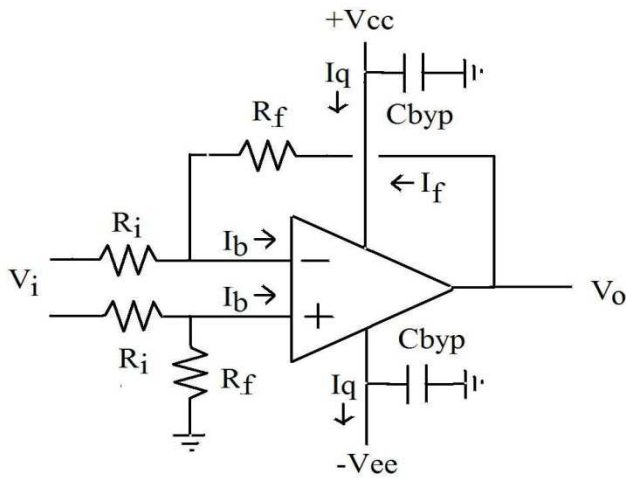
Typical Inverting Mode Circuit
Gain = R_f / R_i

Figure 2



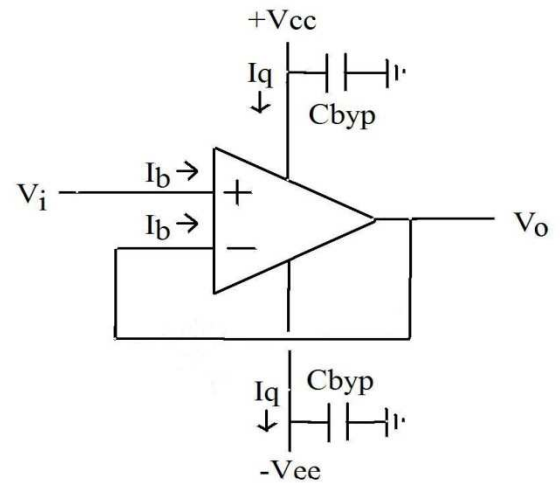
Typical Non Inverting Mode Circuit
Gain = $1 + (R_f / R_i)$

Figure 3



Typical Differential Amplifier Circuit
Gain = R_f / R_i

Figure 4



Unity Gain Buffer Circuit
Gain = +1

Typical Performance Characteristics:

Unless noted, $T_a = 25^\circ\text{C}$, $V_{cc} = \pm 15\text{V}$

Figure 5

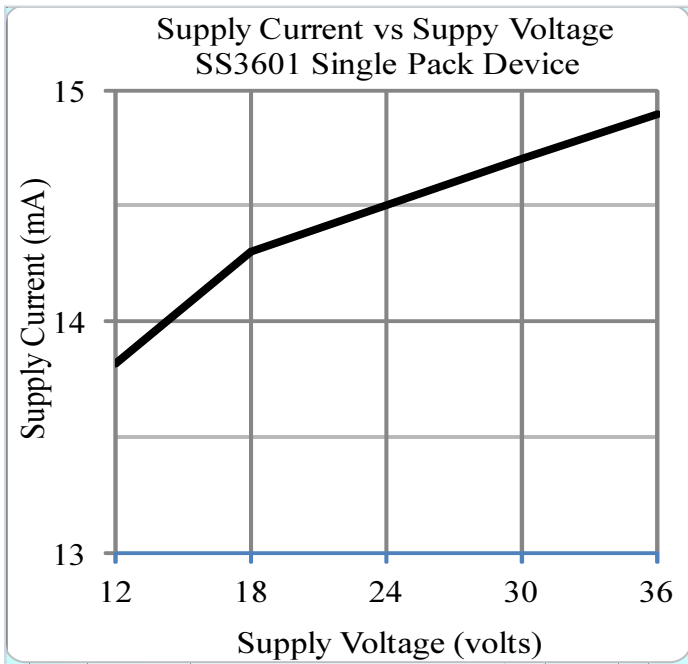


Figure 7

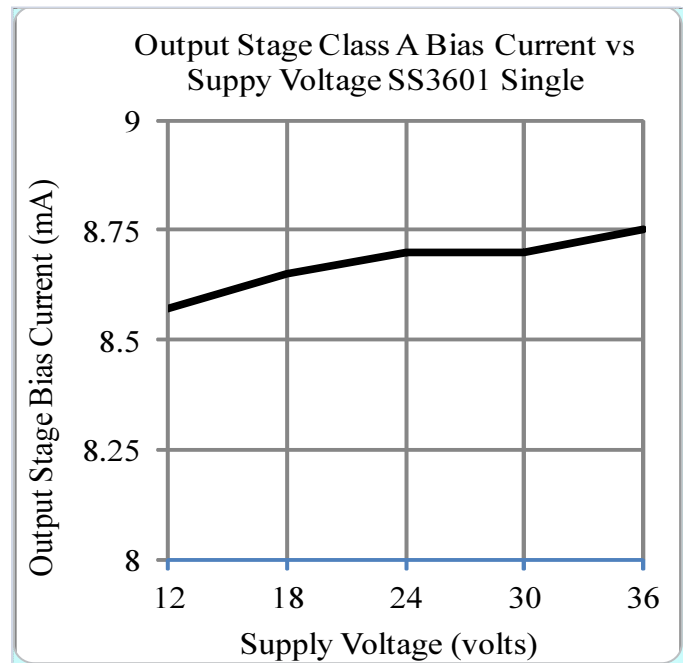


Figure 6

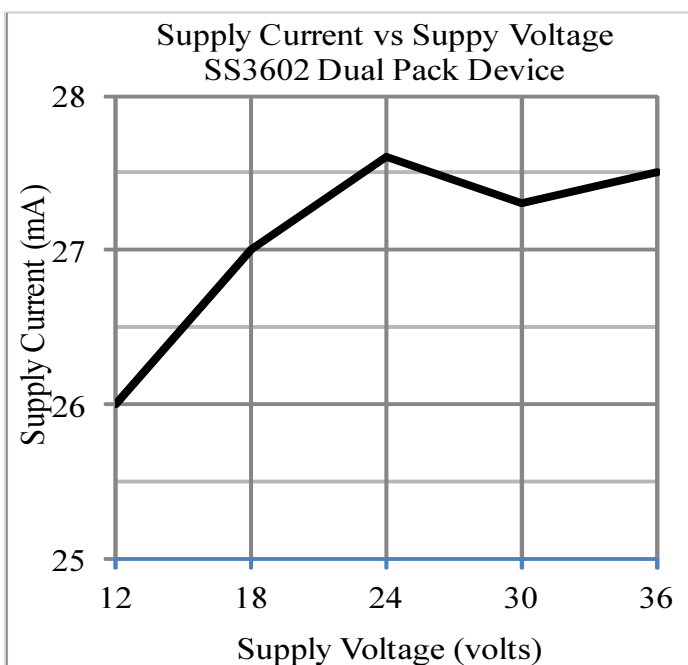


Figure 8

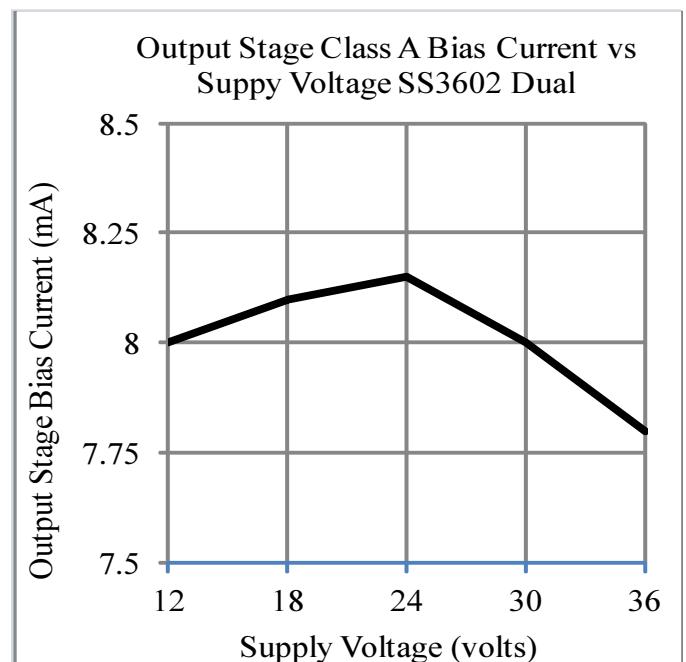


Figure 9

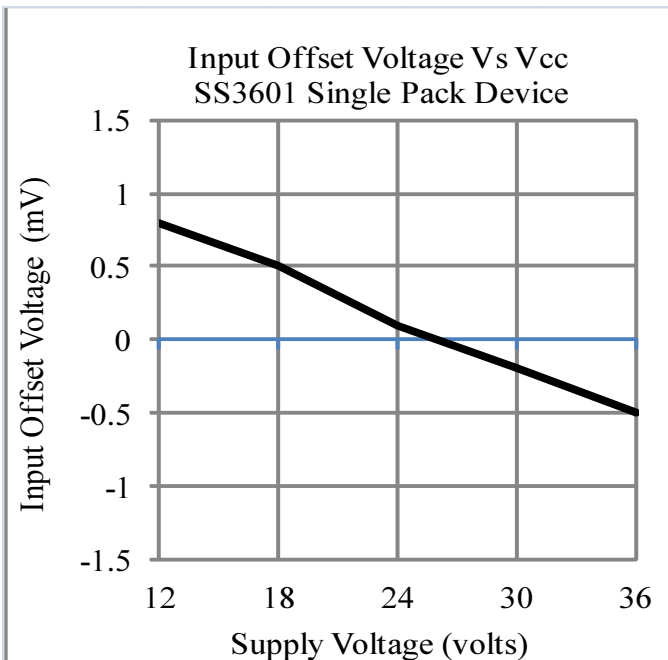


Figure 11 Current Limit Waveform

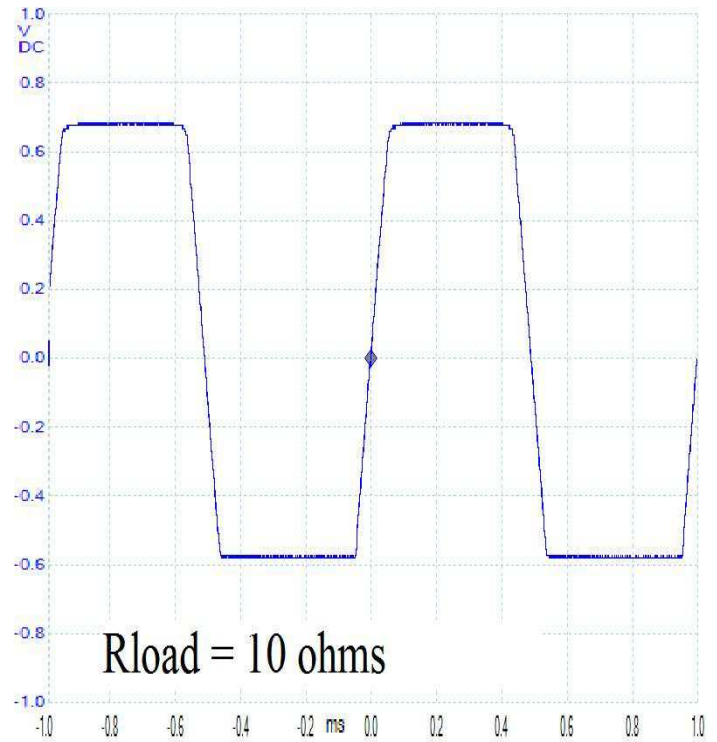


Figure 10

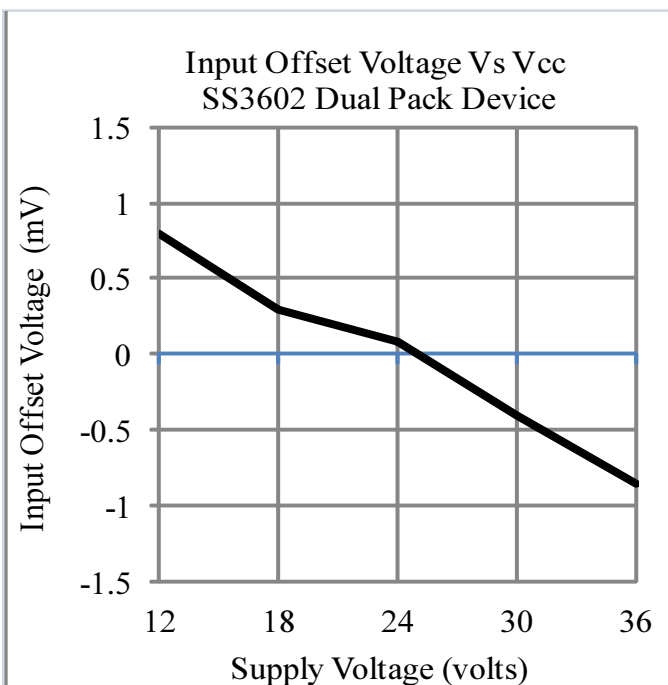


Figure 12 Clipping Waveform

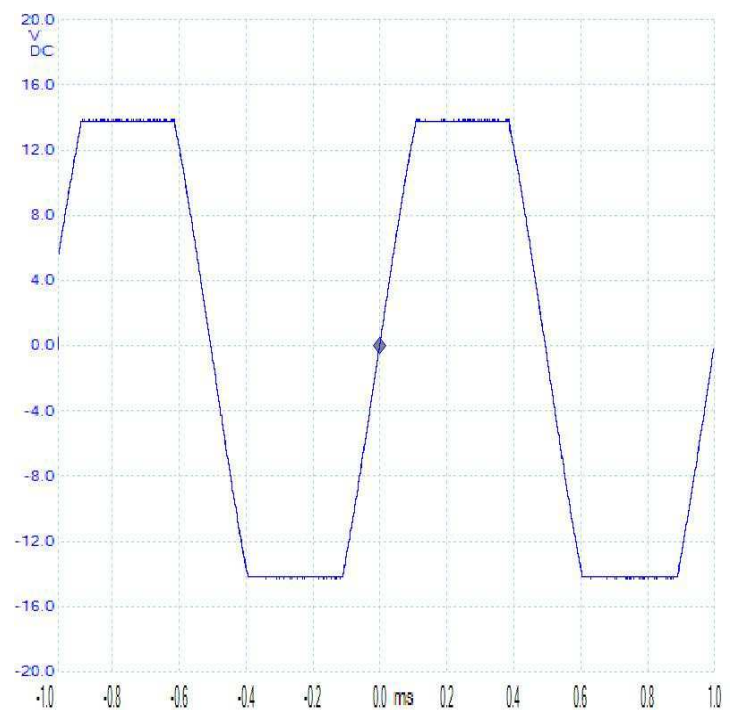


Figure 13 Positive Slewing



Figure 15 Open Loop Gain and Phase

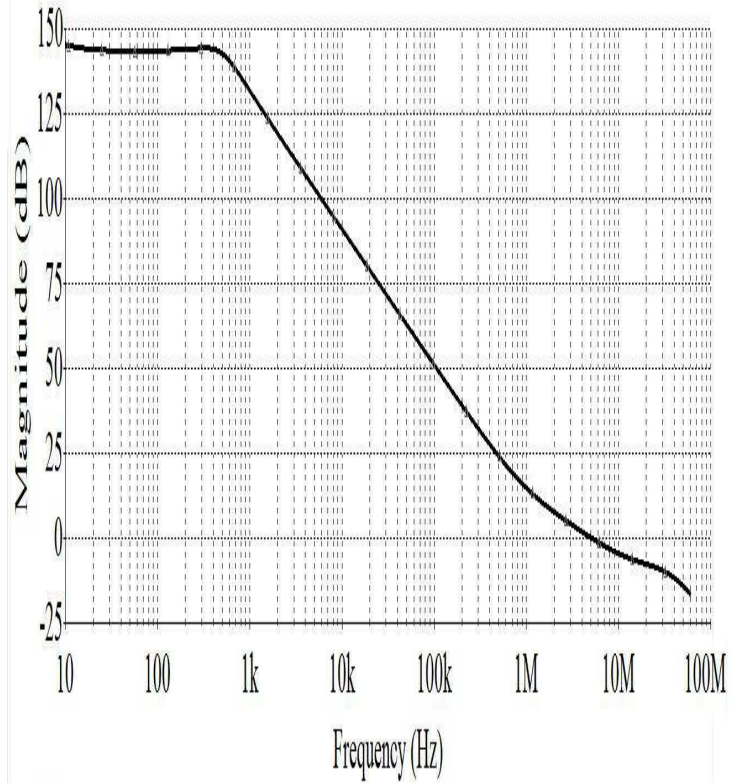


Figure 14 Negative Slewing

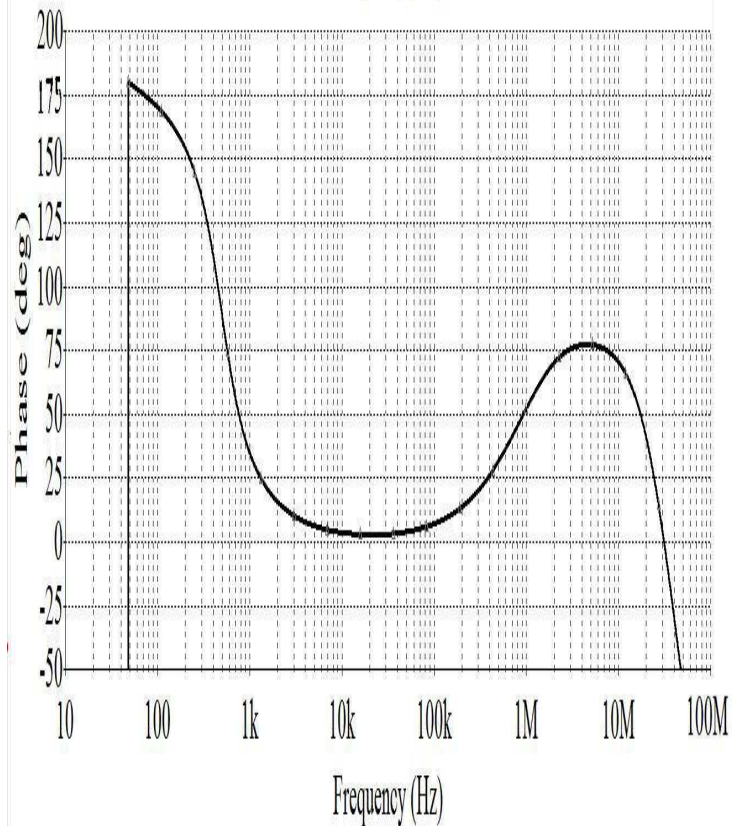
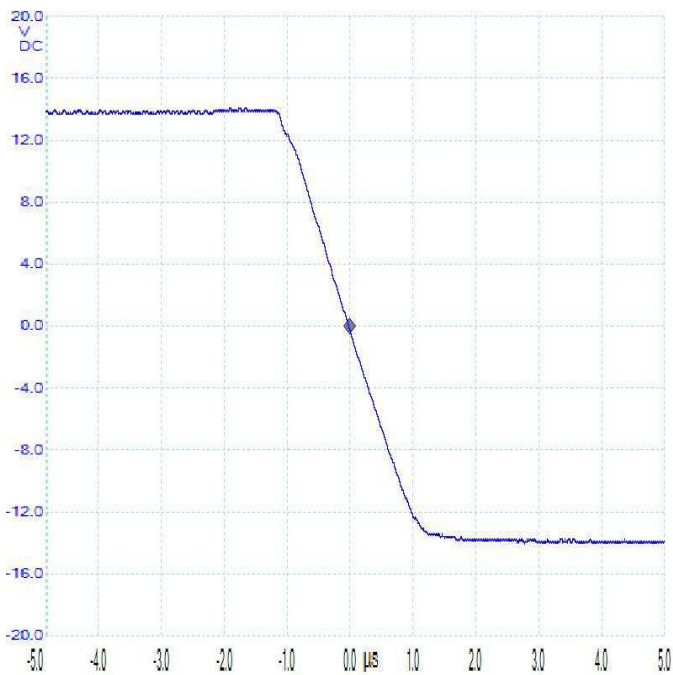


Figure 16 PSRR

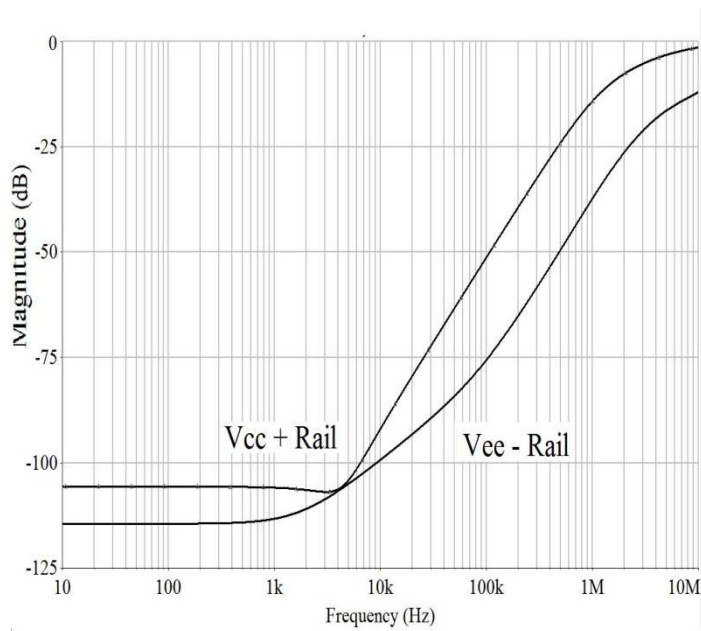
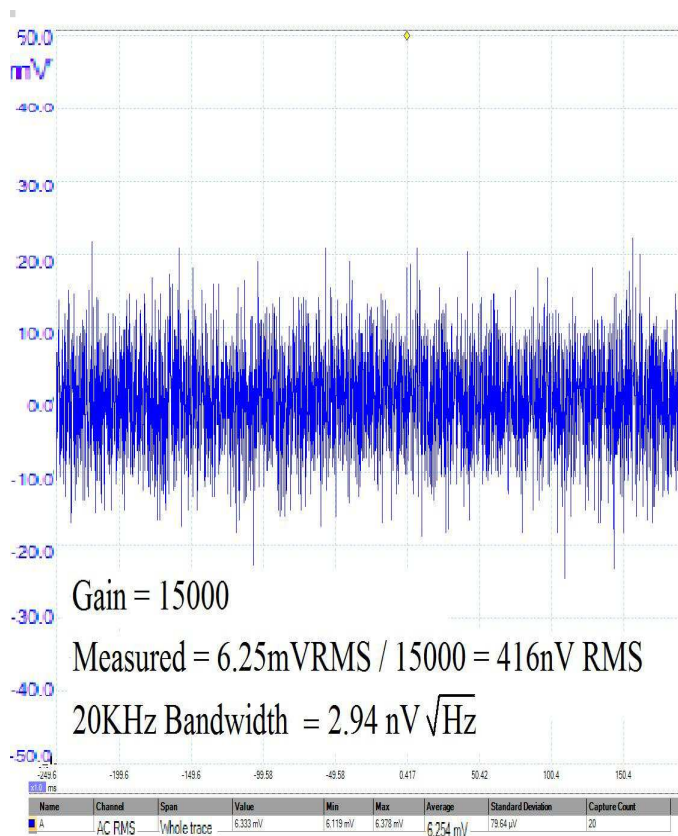


Figure 17 Audio Band Noise



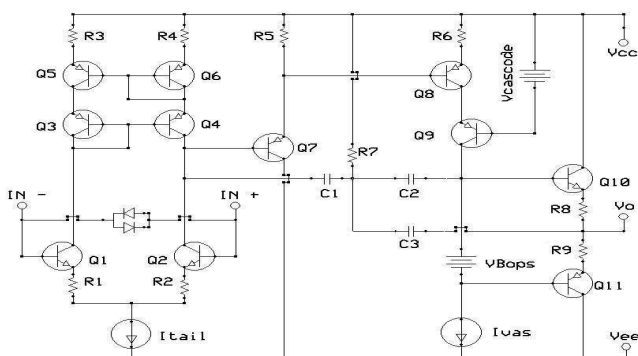
Discrete is Better : The SS3601 / SS3602 discrete op amps will outperform virtually all audio grade monolithic IC op amps in open loop gain, noise performance, output current, and magnitude of class A bias current. Even the coveted OPA627 monolithic op amp, with a price tag of over 25 dollars, has 30dB less gain and around twice the noise of the SS3601 / SS3602. Figure 20 gives a table comparing the SS3601 / SS3602 to a wide array of monolithic op amps.

Discrete designs can afford higher power dissipation, which allows for higher class A bias of the internal circuits and the output stage, as well as much higher available output current than a monolithic design.

Discrete op amps allow for high value NPO / C0G capacitors to be used in elaborate compensation schemes requiring high capacitance capacitors that are impossible to fabricate in monolithics. Since discrete op amps are not fabricated on a single silicon wafer sharing a common substrate, no tradeoffs must be made between the input and output stage transistor characteristics. The SS3601/02 utilizes matched transistor pairs encapsulated within a single device package for the input stage and internal current mirrors - which retains the advantage that monolithics have with device matching.

Theory Of Operation :

Figure 18 Simplified Schematic



Overview: The SS3601 / SS3602 discrete op amp is based on Lin 3 Stage topology consisting of an input stage differential pair, a gain (VAS) stage, and an output stage all biased in class A mode with two pole compensation. All active devices are Bipolar Junction Transistors (BJTs) for the greatest linearity and agility that any silicon device has to offer. The device is fully protected from over current conditions by active current limit circuitry in the output and gain stages, as well as being protected from large differential input voltages by back to back high speed schottky diodes across the inputs. Figure x reveals a simplified schematic, and in reality, the device consists of 17 BJTs, 20 resistors, 3 Capacitors, and a smattering of diodes and precision shunt references.

Input Stage: The input stage of the device is comprised of a dual matched pair of NPN BJTs (Q1 and Q2 in the simplified schematic). This means that the device inputs will pull a small input bias current (specified as I_b) that will flow into the device. The common mode input voltage range of the input stage can be as high as a few volts below the supply rails, however the best performance is obtained by minimizing this to a few volts above and below ground in a split supply application. Input offset voltage is factory trimmed and typically turns out to be better than 300uV @ $\pm 12V_{cc}$. The input stage is protected in the event that the inputs are driven apart, which usually happens during output clipping or rapid slewing. A cascode Wilson current mirror (Q3 - Q6) is utilized as the active load for the input differential pair for precise current matching between the input pair transistors.

Gain (VAS) Stage: The gain stage of the device is a cascode loaded Darlington (Q7 - Q9) for the highest linearity and open loop gain possible. The cascode biasing voltage is derived from precision shunt references, which have a much lower dynamic impedance and lower noise than the low voltage zener diodes which are commonly used

to derive this bias voltage. The Gain stage is current limited by diode clamping action as opposed to a feedback action, which results in greater stability during clip.

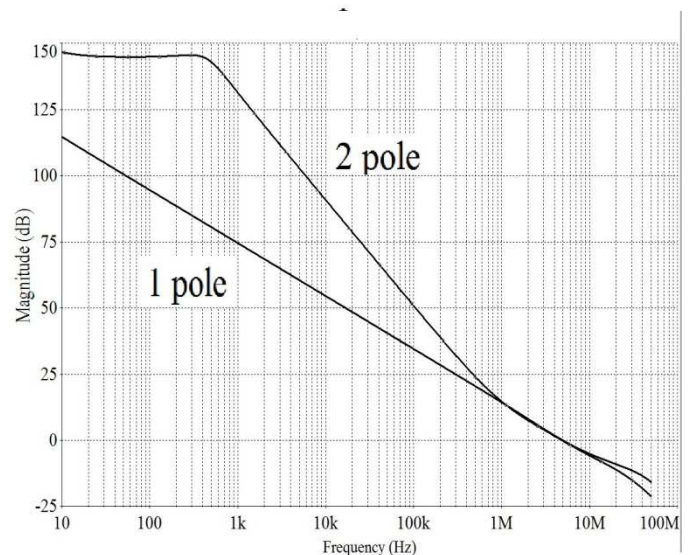
Compensation: The SS3601 / SS3602 employ a uniquely implemented 2 pole compensation scheme that is extremely tolerant of capacitive loading and high feedback network resistance as seen by the input pins. This allows the device to be dropped into virtually any circuit arrangement and work without any stability issues. Such characteristics are usually only obtainable at the expense of slew rate, bandwidth, and open loop gain. Not so with the SS3601 / SS3602.

Upon inspection of the simplified schematic, one can see that some of the compensation is taken from the output stage via C3, and some is taken from the VAS via C2. The value of R7 is small, so the two poles (one formed by C2 and C3, and the other by C1) interact only minimally. This minimal interaction prevents the large gain peak just before roll off that is characteristic of two pole compensation schemes. The low value of R7 also works to minimize the voltage swing across C1, which lightens the load that C1 imposes on the input stage, resulting in greater linearity. As such, the compensation scheme in the device has been dubbed "fractionally output stage inclusive minimally interacting" two pole compensation. The acronym FOSIMI naturally followed, and the only questions now are how to pronounce it and which syllable to emphasize.

Since the VAS only drives a fraction of the compensation capacitance and the output stage drives the rest, the linearity of the VAS is greatly improved. Slew rates also go up, as the slew rate is directly set by the VAS bias current (I_{vas}) and C2. Since the output stage drives the bulk of the compensation capacitance (C2) its value can be large without imposing slew rate limitations on the device.

The device utilizes two pole compensation to ensure that as much open loop gain as possible exists in the audio band. It should be noted that high loop gain acts to correct distortion (THD) when the loop is closed, and that THD tends to rise with falling open loop gain. For a comparison of single pole and two pole compensation, refer to the graph below.

Figure 19 Single Vs Two Pole Comp.



It can be seen that each compensation scheme results in the same open loop bandwidth, but note how much more open loop gain is present at audio frequencies for the two pole scheme compared to the single pole. It is also interesting to note that the pole in the single pole scheme resides in the subsonic region of the curve, resulting in much lower open loop gain within the audio band for single pole compensation. Perhaps worse, is that the input stage must drive the entirety of the current demanded by a single pole network, which greatly degrades its linearity, especially at higher audio frequencies. The 2 pole scheme is implemented such that it will revert back to a single pole rolloff before the loop gain crosses 0 dB as to not compromise Nyquist stability. This can be seen by how the 2 lines converge and overlap starting at about the 15dB / 1 MHz region of the graphs.

2 pole compensation, despite its superiority, is not often used in monolithic op amps due to the difficulty in

fabricating the 2 capacitors at minimum that are required to implement it. Capacitors inside of monolithics consume a large amount of the die area and are therefore kept to a minimum in both capacitor value and quantity. The amount of capacitance required for at least one of the two capacitors in a 2 pole scheme tends to be impossibly large for monolithic designs anyway, even if the die area were available for two capacitors. Being how the SS3601 / 02 employ 3 capacitors for compensation, and since two of them are large (approaching the nF range) these devices would be impossible to fabricate as a monolithic IC.

Monolithic op amps mostly employ single pole compensation schemes. They pay for this by the aforementioned reduction in open loop gain at audio frequencies, as well as a reduction in maximum open loop gain that they can have in the first place. Since compensation schemes burn off gain by nature, and since a single pole scheme burns it off at half of the rate of a two pole scheme, there is a limitation that exists in how much gain they can start out with in the first place to ensure they can burn it all off by the time the phase lag has shifted 180°. The monolithic opamps that DO have a high open loop gain always wind up having an excessively high bandwidth in the 50MHz region or so, which tends to make for a finicky device prone to instability and oscillation. Such high bandwidth devices also suffer from more susceptibility to ill effects from layout parasitics, capacitive loading, resistive feedback networks, and usually require a more stringent power supply bypassing capacitor arrangement comprised of a tantalum and a small value ceramic. Such limitations give most monolithic op amps, even the good ones, little chance of working as drop in replacements.

The compensation capacitors utilized in the SS3601 / SS3602 are high quality NPO dielectric types which have a virtually non-existent voltage coefficient and unmatched stability over temperature variations. When compared to inferior dielectrics such as X7R and Y5V, which can vary in capacitance by 50% over temperature and can change capacitance by 20% with applied voltage, the superiority of the NPO dielectric is clearly evident.

All in all, the SS3601/ SS3602 are compensated to have as much open loop gain as possible that persists for as long as possible, while still having a modest 5 MHz bandwidth, 75° of phase margin, and 10dB of gain margin.

Output Stage: The output stage is a push pull emitter follower biased in class A mode with 8mA of standing current. Due to push pull action, the output stage can source or sink 16mA of current and still remain in class A mode. The output stage will automatically revert to class AB mode in the event that more output current is demanded by the load, however the best THD performance will be obtained by ensuring that the output stage stays in class A mode.

A novel bias control circuit works to servo the output stage bias current to keep it constant across variations in Vcc. Active current limiting is employed in the output stage to protect it from an over current condition. The output transistors are high gain (β) individual devices in a SOT23 package manufactured by Diodes, Inc. who have developed a special manufacturing and encapsulation process that allows their devices to dissipate two to three times the power of a typical SOT23 packaged device. Utilizing these output devices allows the SS3601 / SS3602 to have a high class A bias current and the ability to source or sink far more output current than comparable monolithic op amps in a DIP8 package.

Applications Information:

Bypassing, Grounding, and Layout: The SS3601 / SS3602 discrete op amps require a 0.1 μ F bypass capacitor from each power supply rail to ground for split supply configurations, and across the power supply rails for single supply configurations. These bypass capacitors should be located as close to the device as possible, and connected to the devices Vcc and Vee pins with wide copper traces. This mandatory supply rail bypassing requirement holds true for virtually every op amp in existence. Bypassing the supply rails becomes even more important with high

performance op amps such as the SS3601/SS3602 to ensure proper operation and stability.

Capacitive Loading : Capacitive loading of virtually any op amp ever made will degrade the devices phase margin and Nyquist stability. If the capacitive load is large enough, and the degradation in phase margin is severe enough, the device will oscillate. Buffer / unity gain non inverting configurations, such as the circuit in figure 4, suffer from capacitive loading instability the most while the circuits of figure 1 and 2 are markedly more tolerant. For example, in unity gain buffer mode, the device can direct drive 500pF of load capacitance, but in inverting unity gain mode it can tolerate 2500pF. If one must drive a capacitive load, the cure for any instability that may result is to place some series resistance on the order of 50 ohms in series between the op amps output and the capacitive load.

Feedback Resistor Selection : Feedback resistor values should be kept low to ensure low noise operation. However they should not be so low that they cause the output stage to slip out of class A mode after the load resistance has been factored in. For a design example, consider a unity gain inverting amplifier such as the one in figure 1, that must drive 5V_{peak} into a 1K ohm load. By applying ohms law, one can determine that the load will require 5mA peak to drive. If we arbitrarily decide that we only want to swing ± 10 mA total out of the device, which would allow for around 2.5mA of class A current headroom per output stage half, we can then determine our feedback resistor to be 1K ohms to consume the remaining 5mA of our 10mA output current budget.

It should be noted, that as the equivalent feedback resistance as seen by the input pins rises to around 10 K, stability begins to be compromised as an extraneous pole is being formed against this resistance and the input capacitance of the device. The cure for this potential instability is to place a

small value capacitor (22pF is usually sufficient) in parallel across the feedback resistor; denoted as R_f in figure 1 and 2. This small parallel capacitor ensures that the input pins will see a low impedance at high frequencies, and HF stability will be maintained. It should be noted too, that the addition of this capacitor will limit the closed loop bandwidth to $1 / (2\pi R_f C)$. This is usually inconsequential, as even something as obnoxious as a 100K feedback resistor combined with this 22pF capacitor would only limit the closed loop bandwidth to a snappy 75KHz.

Input Bias and Input Offset : Input offset voltage is dependent upon the device supply voltage. The SS3601 / SS3602 are factory trimmed for input offset voltage with a supply voltage of ± 12 V, which is the center of the supply voltage range. The offset drifts at a rate of 50uV / Volt of supply for the SS3601, and 100uV / Volt of supply for the SS3602. The SS3602 device drifts more because it has 2 PCBs stacked in close proximity to each other, which makes everything vary in temperature more with varying operating conditions.

Input Bias current will also vary slightly with V_{cc} , but typically only ± 300 nA over the entire supply voltage range. It tends to go down when the device is warmer, as the input transistors exhibit a higher hfe with rising temperature.

Drop In Replacement Guide:

The SS3601/SS3602 are drop in replacements for many lower quality op amps provided that the following criteria are met :

1 - The Power supply of the system can provide any extra quiescent current for the SS3601/SS3602 devices over the quiescent current of the op amp being replaced. This is usually not a problem if only a couple of op amps are being replaced, but demands attention if several are being swapped out.

2 - That the replacement op amp circuit does not present an excessively high resistance (>10Kohm) to the input pins. This is usually not a concern either, as most audio circuits tend to use reasonable resistor values in the feedback network to keep noise low. If, however, you find yourself dropping into a high impedance circuit, placing a 22pF capacitor across the feedback resistor (Rf) will cure any instability that may result. See the section called "Feedback Resistor Selection" for more info.

Hopefully, the op amp that is being replaced is in a socket to facilitate easy swap out. If however it is not, then the op amp to be replaced will have to be carefully de-soldered from the PC board from which it resides. It is recommended that one uses solder wick or a vacuum de-soldering pump to assist in solder removal. If no socket existed previously, one can be installed during the swap out procedure without adversely affecting the performance of the SS3601/SS3602

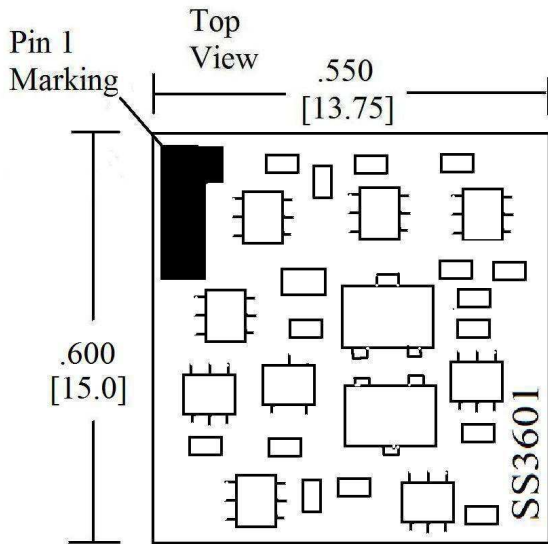
Figure 20 Op Amp Comparison.

DEVICE	GAIN	GAIN @ 10 KHZ	NOISE
SS3601	140 dB	90 dB	3 nV√Hz
OPA2134	120dB	60dB	8 nV√Hz
OPA2604	100dB	65dB	10 nV√Hz
OPA627	116dB	63dB	4.5 nV√Hz
OPA134	120dB	60dB	8 nV√Hz
OPA1642	134dB	60dB	5.1 nV√Hz
LM833	110dB	68dB	4.5 nV√Hz
NE5532	100dB	67dB	5 nV√Hz
LME49723	116dB	60dB	3.6 nV√Hz
AD8066	113dB	77dB	7 nV√Hz
AD712	112dB	?	16 nV√Hz
AD8620	105dB	65dB	6 nV√Hz
MUSES01	105dB	?	9.5 nV√Hz
LF353	100dB	?	18 nV√Hz
RC4580	110dB	?	4.6 nV√Hz
TL072	106dB	?	18 nV√Hz

? = Unspecified

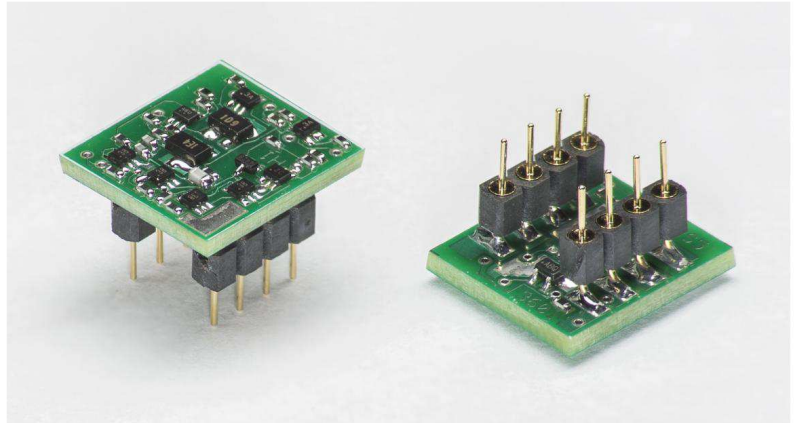
Mechanical And Packaging Data :

SS3601 Single Pack Device

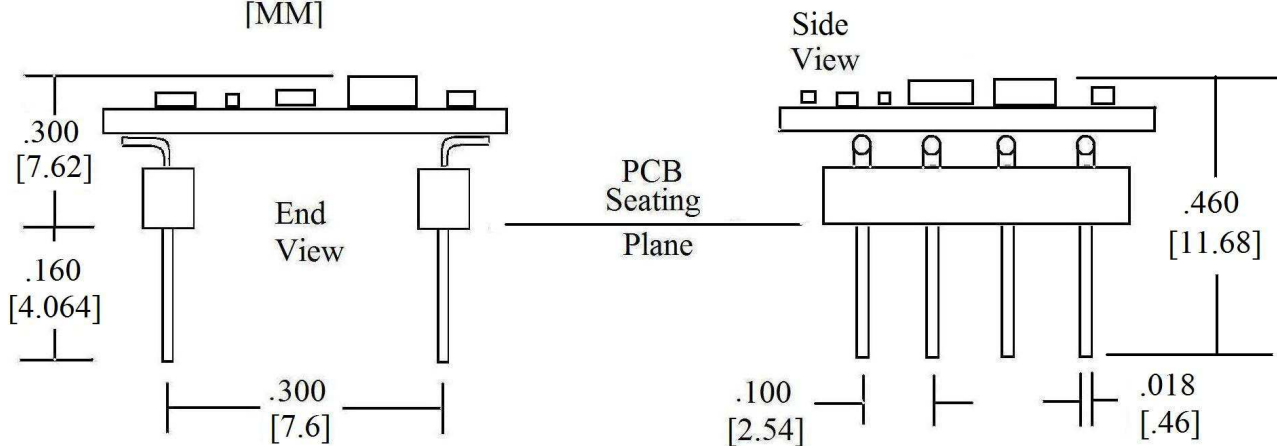


Not To Scale
Dimensions are in
Inches
[MM]

SS3601 Single Discrete Op Amp Mechanical Data



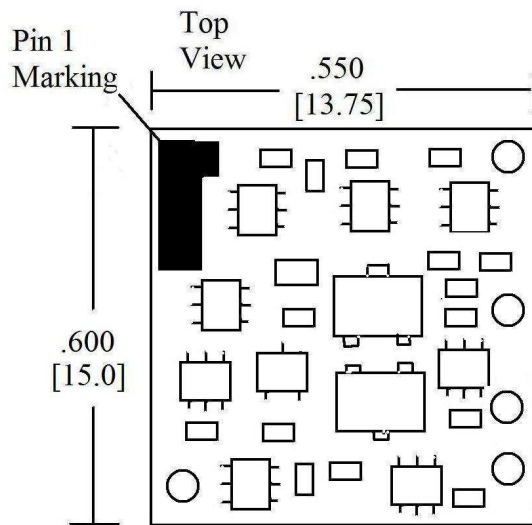
Pin Pitch And Row Spacing
Are Equal To That Of A DIP 8



Pins Are Circular Machined Gold Plated
Fits any DIP socket

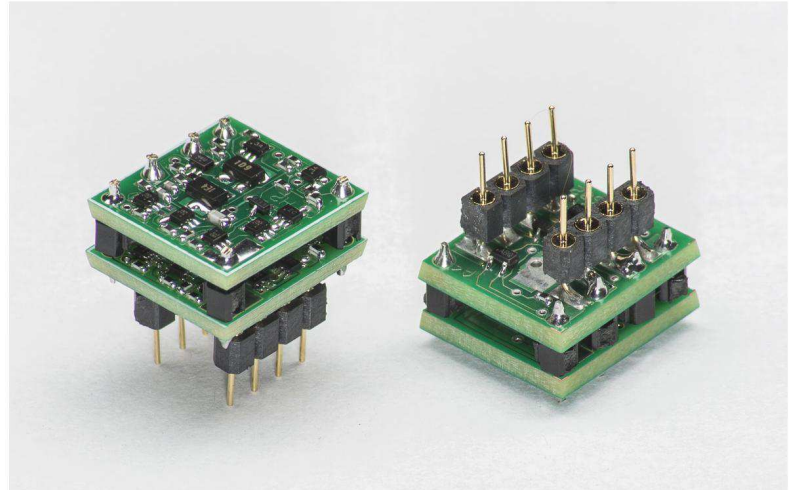
Mechanical And Packaging Data :

SS3602 Dual Pack Device

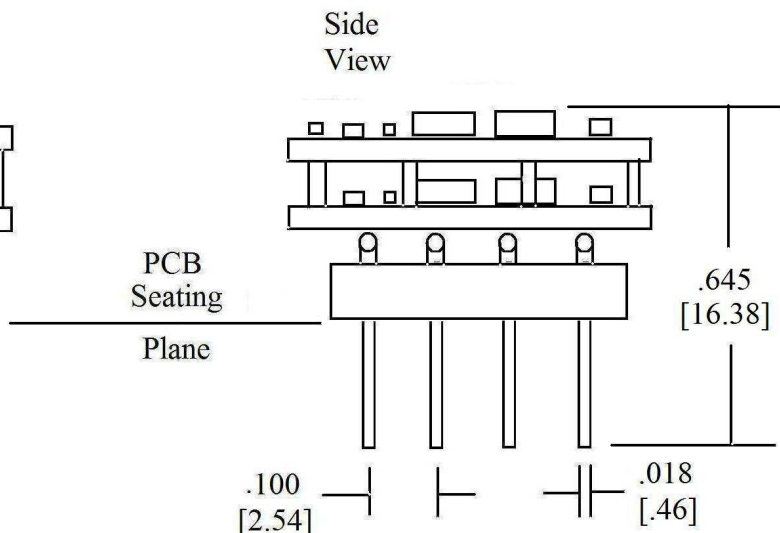
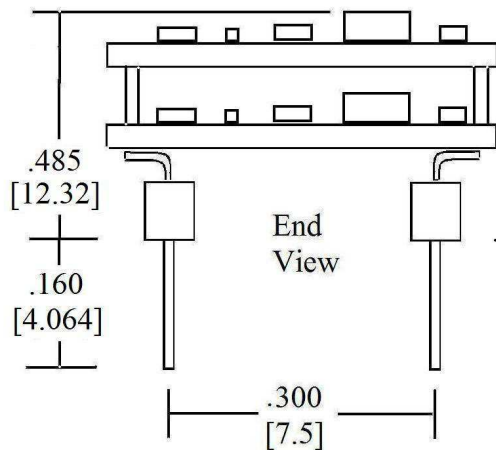


Not To Scale
Dimensions are in
Inches
[MM]

SS3602 Dual Discrete Op Amp Mechanical Data



Pin Pitch And Row Spacing
Are Equal To That Of A DIP 8



Pins Are Circular Machined Gold Plated
Fits any DIP socket

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