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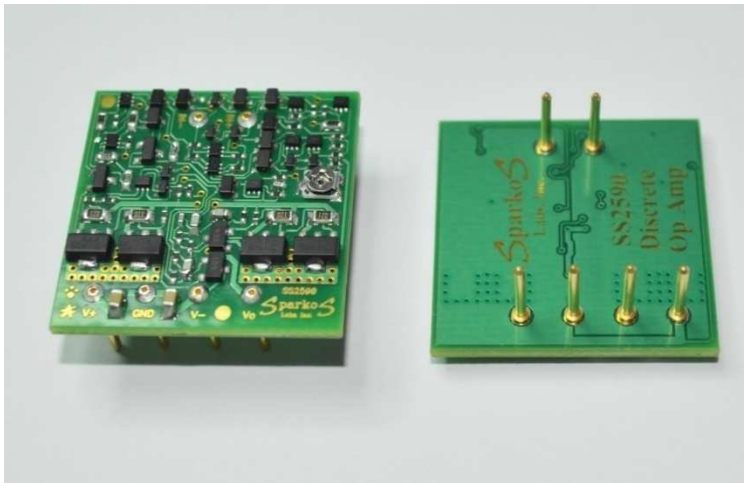
SS2590 Discrete Op Amp

Description :

The SS2590 discrete op amp is designed to be the ultimate op amp for use in studio and pro audio applications.



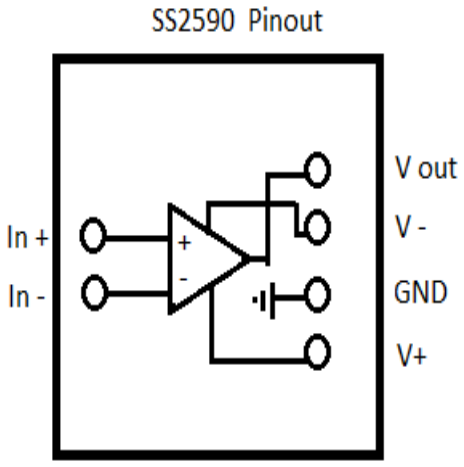
Features:

- **165 dB Open Loop Gain to 100 Hz**
- **Two Pole Compensation**
- **10MHz Unity Gain Bandwidth**
- **Class A Output Current Of +/- 32mA**
- **Maximum Output Current Of +/- 250mA**
- **1.5nV√Hz noise in a 20KHz bandwidth**
- **Less than 1mV Offset**
- **On-Board Supply Decoupling Caps**
- **Able to drive 75 ohm loads at full power**
- **+/-9V to +/-24V supply voltage range**
- **All BJT design with input bias current cancellation**
- **Unity gain stable**
- **Fully Discrete Design**

Compatible with:

- **Automated Processes API2520, API2525**
- **Jensen and John Hardy 990 series**
- **Sound Skulptor SK series**
- **Purple Audio KDJ series**
- **Five Fish Studio Discrete series**
- **Avedis Audio 1122**
- **Seventh Circle Audio SC series**
- **Yamaha NE series**
- **Rogue 5 series discrete op amps**
- **Whistle Rock Audio series**
- **Warm Audio discrete series**

Pin Assignment :



Absolute Maximum Ratings

Exceeding the Aboslute Maximum Ratings could result in permanent damage to the device. These ratings are absolute maximum, and are not recommended for normal operation.

Symbol	Parameter	Conditions	Rating	Unit	Notes
Vcc	Supply Voltage	Single Supply	60	V	
		Split Supply	±30		
Vdiff	Sustained Differential Input Voltage		680	mV	4
Vcm	Common Mode Input Voltage		Vcc to Vee	V	
Iin	Input Current	+ or - op amp input	50	mA	4
Io	Output Current	Short to Ground	275	mA	1 , 2
		Short to Vcc or Vee	275	mA	1 , 3
Top	Operating Ambient Temperature		-25 to +70	˚C	
Tstg	Storage Temperature		-40 to +120	˚C	

Notes:

1 The output current is internally limited
2 Short circuits to ground can be maintained indefinately
3 Short circuits to Vcc or Vee may damage the device by overheating if they are prolonged for several seconds
4 The input pins are clampped with back to back (anti parallel) schottkey diodes.

DC Characteristics

Unless otherwise noted, Ta = 25˚C, Vcc = +18V, Vee = - 18V, Vcm = 0

Symbol	Paramater	Conditions	Min	Typ	Max	Units	Notes
Vcc	Supply Voltage	Single Supply	18	36	48	V	
		Split Supply	±9	±18	±24	V	
Iq	Quiescent Current		22	25	28	mA	
Ignd	Ground Pin Current			0		mA	
Vos	Input Offset Voltage			±300	±600	µV	
Vcm	Common Mode Input Voltage		Vee + 3		Vcc - 3	V	
Ib	Input Bias Current			0.2	1.5	µA	
Io	Output Current	Class A Mode		32		mA	1
		Class AB Mode		250		mA	2
		Current Limit		260	275	mA	

Notes:

1 This is the Max Io that the output stage can swing while remaining in class A mode
2 This is the Max Io that the ouput stage can swing without entering current limit

AC Characteristics

Unless otherwise noted, Ta = 25˚C, Vcc = +18V, Vee = - 18V, Vcm = 0

Symbol	Paramater	Conditions	Min	Typ	Max	Units	Notes
Aol	Open Loop Gain			165		dB	1
SR	Slew Rate	Positive Direction		18		V/µS	
		Negative Direction		15		V/µS	
Vo max	Maximum Output Voltage	@ Rload = 5K ohm	Vee+2.5		Vcc-2.5		3
		@ Rload = 75 ohm	Vee+3.5		Vcc-3.5		
Cl	Capacitive Load Drive	Figure 1 or 2, Av = -1 or +2		3000		pF	2
Cl	Capacitive Load Drive	Figure 4, Av = +1		330		pF	2
BW	Unity Gain Bandwidth			10		MHz	1
θm	Phase Margin	@ Unity gain Crossover		65		˚	1
en	Voltage Noise Density	DC - 20 KHz Bandwidth		1.5		nV/√Hz	
N	Broad Band Noise	DC - 20 KHz Bandwidth		210		nV RMS	
Cin	Input Capacitance			5		pF	

Notes

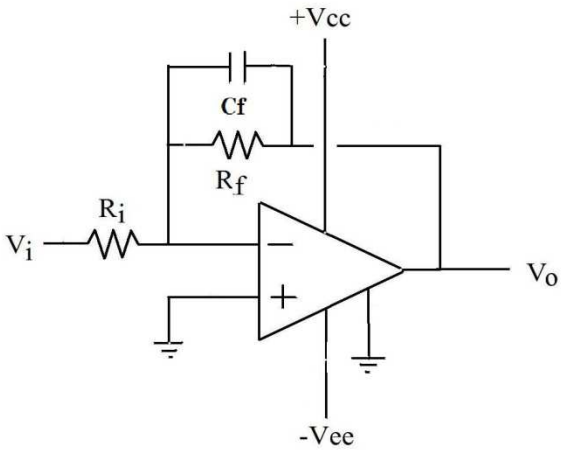
1 A plot of Open Loop Gain and Phase across frequency can be found in the Typical Performance Characteristics section of this datasheet.

2 This specification does not apply to capacitors inside of the external feedback loop, such as in filter circuits, as these will not affect stability.

3 Cascode structures inside of the device will begin to debias when the outupt swing approaches 3.5V away from either supply rail. This is non destructive, and the output will not visibly clip, however there will be a ~25dB reduction in open loop gain, resulting in higher THD.

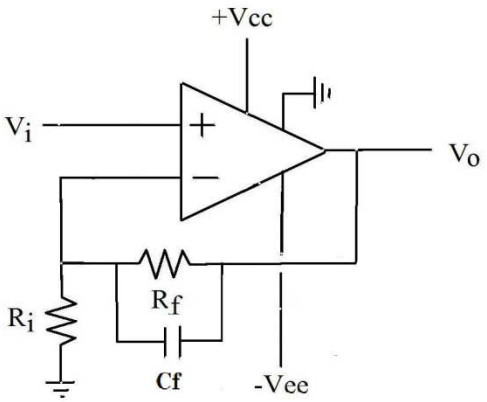
Application Circuits

Figure 1



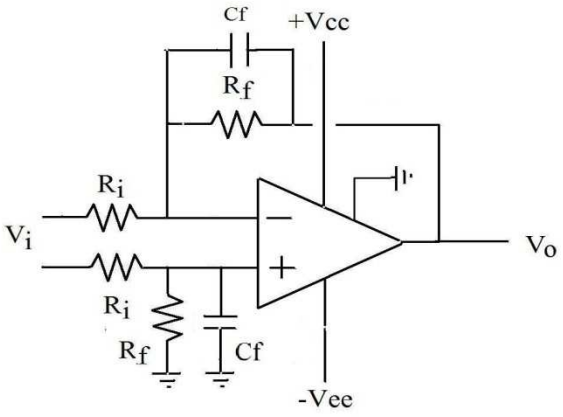
Typical Inverting Mode Circuit
Gain = Rf / Ri
Bandwidth = 1 / (2 pi Rf Cf)

Figure 2



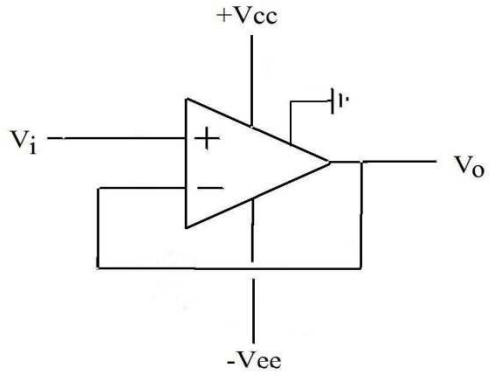
Typical Non Inverting Mode Circuit
Gain = 1 + (Rf / Ri)
Bandwidth = 1 / (2 pi Rf Cf)

Figure 3



Typical Differential Amplifier Circuit
Gain = Rf / Ri

Figure 4



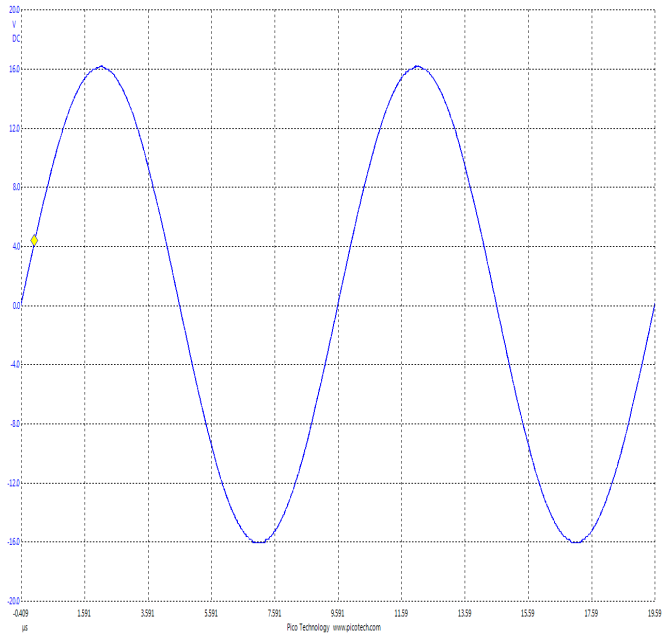
Unity Gain Buffer Circuit
Gain = +1

Typical Performance Characteristics:

Unless noted, Ta = 25˚C, Vcc = ±18V

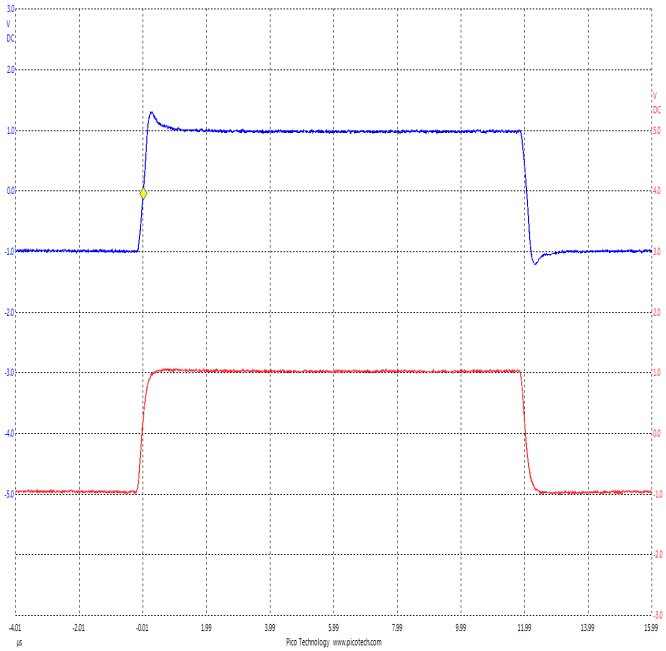
100KHZ full power Sign Wave:

2uS/DIV, 4V/DIV, Rl = 75 ohms, Vcc = +/-24V, Gain = 2.5 Vcc = +/-20V



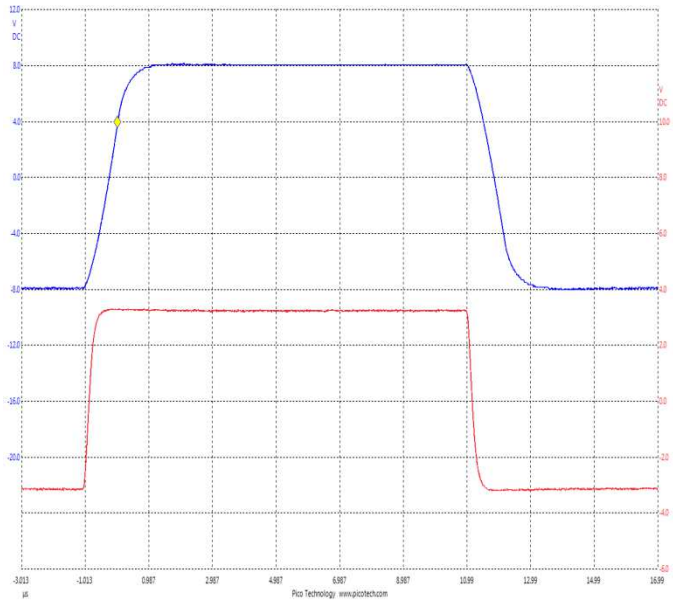
Small Signal Pulse Response:

2uS/DIV, 1V/DIV, Red = Input, Blue = output, Rl = 75 Ohms, Gain = +1.



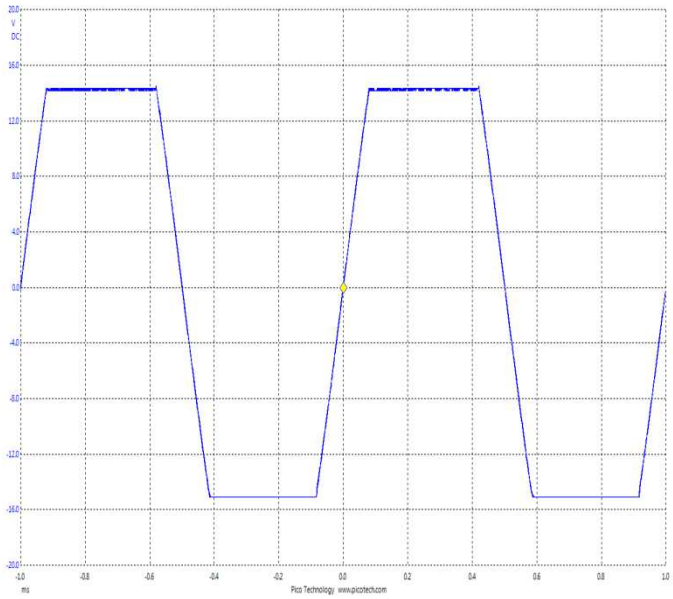
Large Signal Pulse Response:

2us/DIV, Red = Input, 2V/Div, Blue = Output, 4V/DIV, Rl = 75 ohms, Gain = +2.5

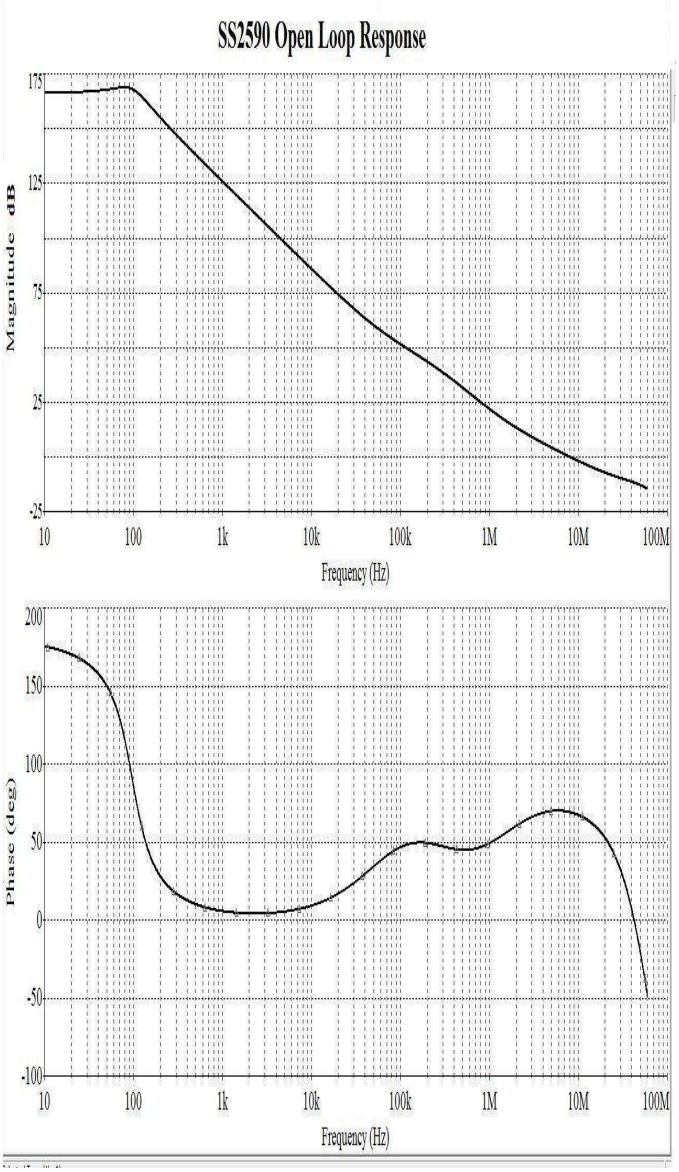


Clipping Waveform :

200uS/DIV, 4V/DIV, Rl = 75Ohms



Open Loop Gain And Phase :



The SS2590 : After the success of the SS3601 / SS3602 discrete op amps we turned our attention to the discrete op amps that are found in studio gear and recording equipment such as the API2520 and Jensen 990 style devices. Numerous devices that are compatible with these exist on the market, and after buying and evaluating a hand full of them we decided that we could do better. Much better.

The first thing that we noticed upon evaluating some devices in this class was that most of them are manufactured with archaic, decades old through-hole components. This is not so bad in and by its self, (aside from component lead inductance) but the problem with them is that most of these through-hole components (especially the transistors) are old, slow, and pale in comparison to modern devices. The SS2590 makes use of the highest speed and highest gain transistors available. We use 300MHz rated output transistors while everyone else is using devices in the 20 to 50 MHz region.

Two Pole Compensation : We're the only ones doing this. Two Pole Compensation is the ultimate compensation technique for maximizing open loop gain within the audio bandwidth. High open loop gain makes for a more precise amplifier, lower THD performance, and keeps the slew rates high, which makes for more natural attacks and transients.

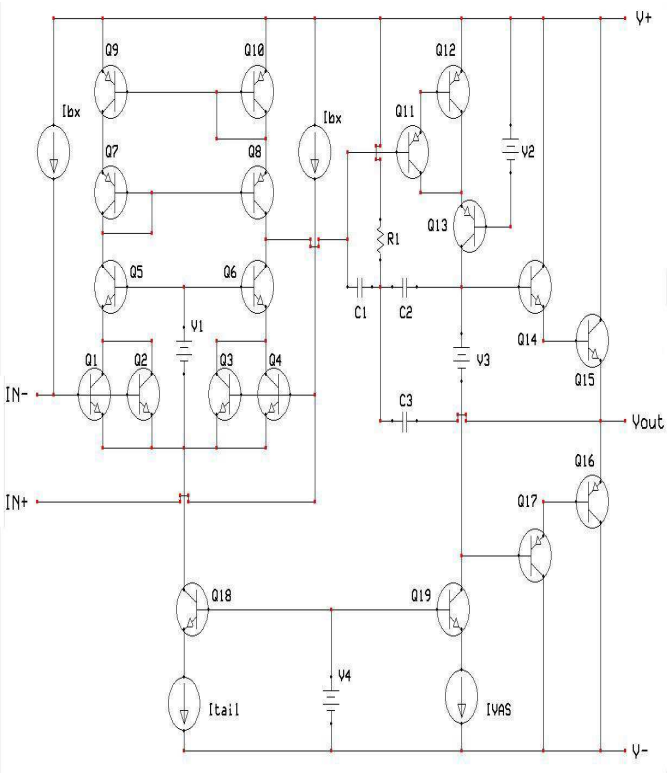
We found the noise performance of the majority of the discrete op amps in this class to be abysmal; measuring in at several nv√Hz in most designs. Some of the better devices specified in the 1 to 1.5 nv√Hz range, but they all seemed to achieve this noise performance by putting shunt inductors across the RE resistors in the input stage which "shorts out" the RE resistors and eliminates their noise contribution. While this technique yields lower noise, it does so at the expense of input stage linearity since the linearizing affect of the RE resistors are lost by the shorting inductors. RE resistors in the input stage are a good thing, and will linearize the input stage by swamping the non-linear Rbb of the input stage transistors. On the SS2590, we opted to keep the input stage RE resistors in order to reap their associated linearity benefit, and we reduced the noise back down by paralleling the input transistors. It's the best of both worlds, with the only drawback being a slight increase in input stage complexity.

The DC precision of the devices that we evaluated left something to be desired as well. We saw offsets in the double digit mV range with warm-up drifts of several mV more. The SS2590 has a built in POT to allow precise offset adjustment and it has a warm up drift of less than 1mV. Input bias current induced offsets are greatly reduced by using on board current sources to supply

the input bias current for the device. This keeps the SS2590 from pulling input bias current from the outside world and creating offsets against the resistances seen by the input pins.

Theory Of Operation :

Simplified Schematic



Overview: The SS2590 discrete op amp is based on Lin 3 Stage topology consisting of an input stage differential pair, a gain (VAS) stage, and an output stage all biased in class A mode with two pole compensation. All active devices are Bipolar Junction Transistors (BJTs) for the greatest linearity and agility that any silicon device has to offer. The input stage and gain stage are all cascoded and biased from cascoded current sources. This architecture yields a very high open loop gain and has unparalleled bias current stability across power supply and operational variances. The device is fully protected from over current conditions by active current limit circuitry in the output and gain stages, as well as being protected from large differential input voltages by back to back high speed schottky diodes across the inputs. The simplified schematic can be found to the right, and in reality, the device consists of 35 BJTs, 37 resistors, 7 Capacitors, and a smattering of diodes and precision shunt references.

Input Stage: The input stage of the device is comprised of 2 pairs of cascoded dual matched NPN BJTs (Q1 - Q4 in the simplified schematic). This input pair arrangement using multiple input transistors in parallel reduces the noise of the input stage to an astonishingly low 1.5nV√Hz across the audio band. Input bias current cancellation is used (Ibx in the simplified schematic) to reduce input bias current induced offsets that can occur when BJT input stages are used. Input offset voltage is factory trimmed with the on board POT and typically turns out to be better than 300uV @ ±18Vcc. The input stage is protected in the event that the inputs are driven apart, which usually happens during output clipping or rapid slewing. A cascode Wilson current mirror (Q7 - Q10) is utilized as the active load for the input differential pair for precise current matching between the differential pair halves.

Gain (VAS) Stage: The gain stage of the device is a cascode loaded Darlington (Q11 - Q13) for the highest linearity and open loop gain possible. The cascode biasing voltage (V2) is derived from precision shunt references, which have a much lower dynamic impedance and lower noise than the low voltage zener diodes which are commonly used to derive this bias voltage. The gain stage is current limited by diode clamping action as opposed to a feedback action, which results in greater stability during clip.

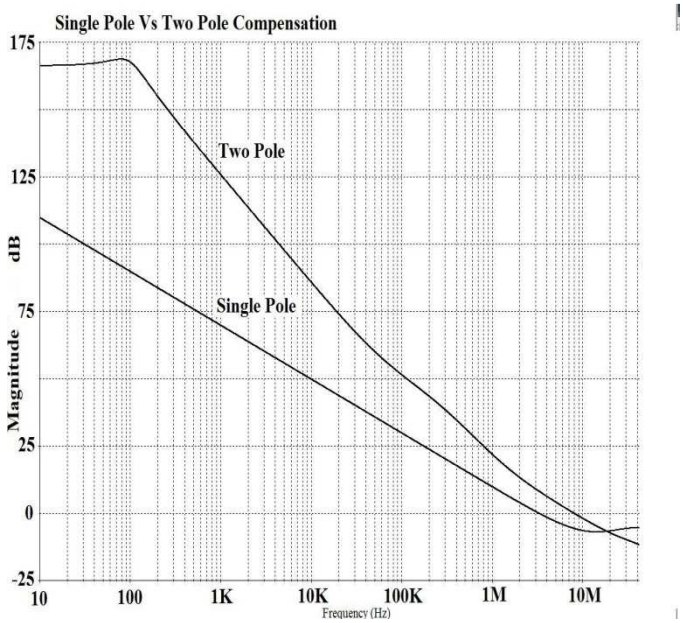
Compensation: The SS2590 employs a uniquely implemented 2 pole compensation scheme

that yields the highest open loop gain possible that persists as long as possible throughout the audio bandwidth.

Upon inspection of the simplified schematic, one can see that some of the compensation is taken from the output stage via C3, and some is taken from the VAS via C2. The value of R1 is small, so the two poles (one formed by C2 and C3, and the other by C1) interact only minimally. This minimal interaction prevents the large gain peak just before roll off that is characteristic of two pole compensation schemes. The low value of R1 also works to minimize the voltage swing across C1, which lightens the load that C1 imposes on the input stage, resulting in greater linearity. Since the VAS only drives a fraction of the compensation capacitance and the output stage drives the rest, the linearity of the VAS is greatly improved. Slew rates also go up, as the slew rate is directly set by the VAS bias current (Ivas) and C2. Since the output stage drives the bulk of the compensation capacitance (C3) its value can be large without imposing slew rate limitations on the device.

Using two pole compensation ensures the highest open loop gain that is possible exists in the audio band. It should be noted that high loop gain acts to correct distortion (THD) when the loop is closed, and that THD tends to rise with falling open loop gain. For a comparison of single pole and two pole compensation, refer to the following plot:

Single Vs Two Pole Comp.



It can be seen that each compensation scheme results in roughly the same open loop bandwidth, but note how much more open loop gain is present at audio frequencies for the two pole scheme compared to the single pole. It is also interesting to note that the pole in the single pole scheme resides in the subsonic region of the curve, resulting in much lower open loop gain within the audio band for single pole compensation. Perhaps worse, is that the input stage must drive the entireity of the current demanded by a single pole network, which greatly degrades its linearity, especially at higher audio frequencies. The 2 pole scheme is implemented such that it will revert back to a single pole rolloff before the loop gain crosses 0 dB as to not comporomise Nyquist stability.

Output Stage: The output stage is a darlington push pull emitter follower biased in class A mode with 16mA of standing current. Due to push pull action, the output stage can source or sink 32mA of current and still remain in class A mode. The output stage will automatically revert to class AB mode in the event that more output current is demanded by the load, however the best THD performance will be obtained by ensuring that the output stage stays in class A mode.

A novel bias control circuit works to servo the output stage bias current to keep it constant

across variations in Vcc and temperature. Active current limiting is employed in the output stage to protect it from an over current condition.

There are large copper areas underneath the PCB that the output stage utilizes as a heat sink. As such, no heat sink is required.

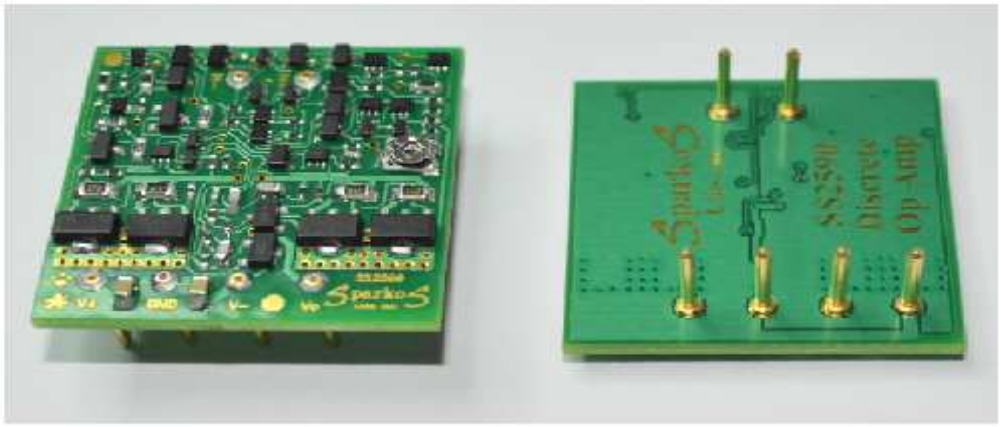
Applications Information:

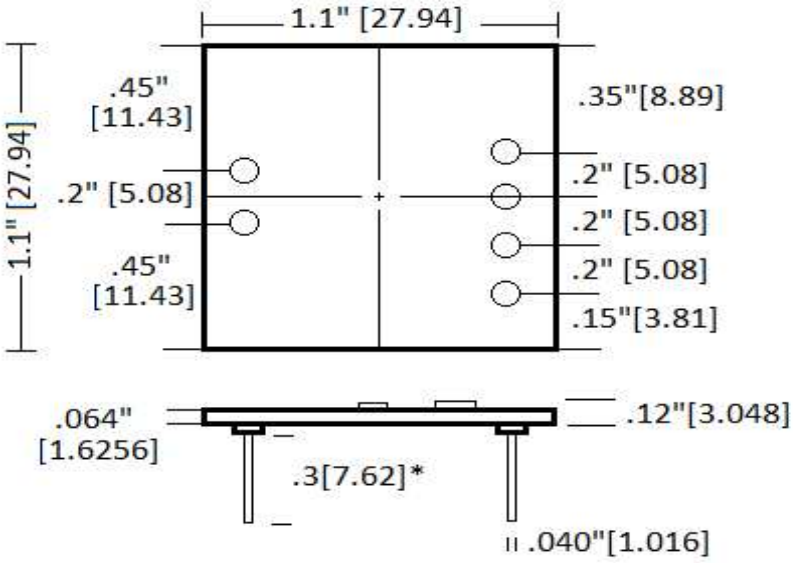
Bypassing, Grounding, and Layout: The SS2590 discrete op amp has two power supply bypass capacitors on-board from VCC to GND, and VEE to GND. As such, these power supply bypass capacitors are not required externally. The only use for the Ground pin of the device is for these bypass capacitors. As such, the ground pin will have no DC current flowing in it.

Capacitive Loading : Capacitive loading of virtually any op amp ever made will degrade the devices phase margin and Nyquist stability. If the capacitive load is large enough, and the degradation in phase margin is severe enough, the device will oscillate. Buffer / unity gain non inverting configurations such as the circuit in figure 4 suffer from capacitive loading instability the most while the circuits of figure 1 and 2 are markedly more tolerant. For example, in unity gain buffer mode, the device can direct drive 330pF of load capacitance, but in inverting unity gain mode it can tolerate 3000pF. If one must drive a capacitive load, the cure for any instability that may result is to place some series resistance on the order of 50 ohms in series between the op amps output and the capacitive load.

Mechanical And Packaging Data :

SS2590 Discrete Op Amp





*longer pins are available

Dimensions are in Inches [MM]

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